4-Mbit (256K x 16) Static RAM

Features

- **Temperature Ranges**
  - — **Industrial**: **–40°C to +85°C**
  - — **Automotive-A: –40°C to +85°C**
  - — **Automotive-E: –40°C to +125°C**
- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62147CV25, CY62147CV30, and CY62147CV33**
- **Ultra-low active power**
  - — **Typical active current: 1.5 mA @ f = 1 MHz**
  - — **Typical active current: 8 mA @ f = f_{max}**
- **Ultra low standby power**
- **Easy memory expansion with $\overline{CE}$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball VFBGA and non Pb-free 44-pin TSOPII**
- **Byte power-down feature**

Functional Description[1]

The CY62147DV30 is a high-performance CMOS static RAM organized as 256K words by 16 bits. This device features ad-vanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode reducing power consumption by more than 99% when deselected (CE HIGH or both BLE and BHE are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{17}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{17}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table at the back of this data sheet for a complete description of read and write modes.

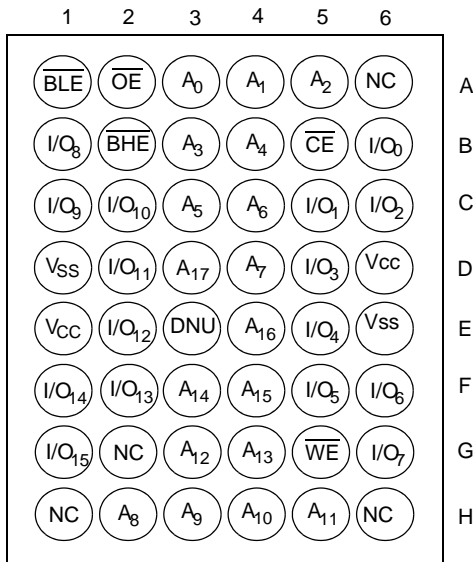The CY62147DV30 is available in a 48-ball VFBGA, 44 Pin TSOPII packages.
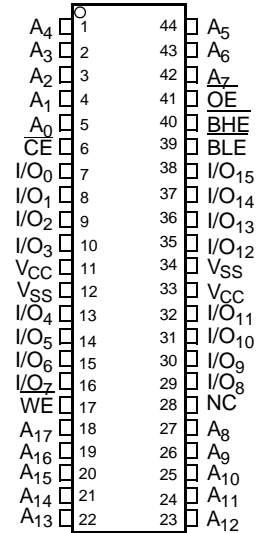
Logic Block Diagram
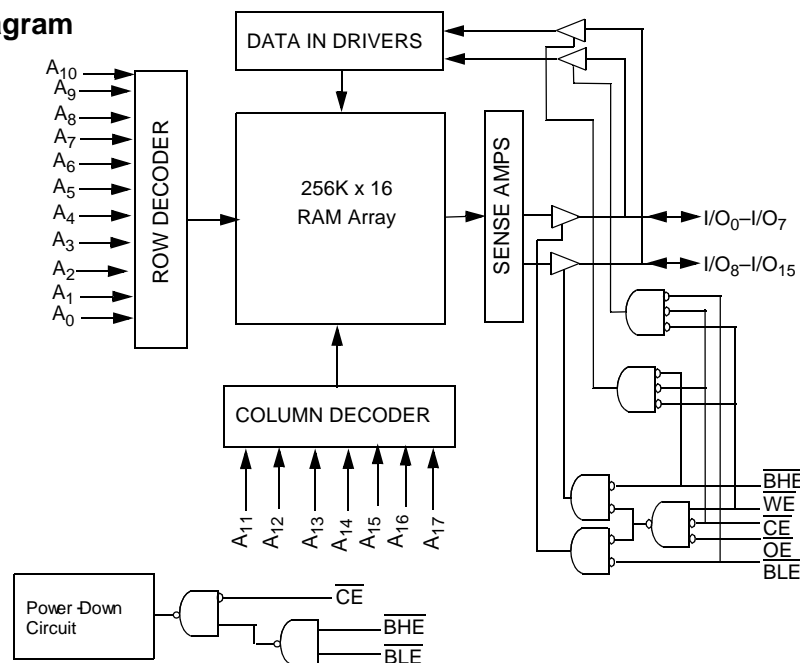
Note:
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

[+] Feedback

Pin Configuration[2, 3, 4]

VFBGA (Top View)

44 TSOP II (Top View)

Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (μA)	
						f = 1MHz		f = f_{max}			
		Min.	Typ.[5]	Max.		Typ.[5]	Max.	Typ.[5]	Max.	Typ.[5]	Max.
CY62147DV30LL	Industrial	2.2V	3.0	3.6	45	1.5	3	10	20	2	8
CY62147DV30LL	Industrial	2.2V	3.0	3.6	55	1.5	3	8	15	2	8
CY62147DV30L	Auto-E										25
CY62147DV30LL	Industrial	2.2V	3.0	3.6	70	1.5	3	8	15	2	8
CY62147DV30LL	Auto-A										8

Notes:
2. NC pins are not internally connected on the die.
3. DNU pins have to be left floating or tied to V_{SS} to ensure proper application.
4. Pins H1, G2, and H6 in the VFBGA package are address expansion pins for 8 Mb, 16 Mb, and 32 Mb, respectively.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.

[+] Feedback

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ....–65°C to +150°C

Ambient Temperature with
Power Applied..–55°C to +125°C

Supply Voltage to Ground
Potential ....–0.3V to + $V_{CC(MAX)}$ + 0.3V

DC Voltage Applied to Outputs
in High-Z State[6,7]..........................–0.3V to $V_{CC(MAX)}$ + 0.3V

DC Input Voltage[6,7] .... –0.3V to $V_{CC(MAX)}$ + 0.3V

Output Current into Outputs (LOW)............................ 20 mA

Static Discharge Voltage... >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current... >200 mA

Operating Range

Device	Range	Ambient Temperature $[T_A]$[9]	V_{CC}
CY62147DV30L	Automotive-E	–40°C to +125°C	2.20V to 3.60V
CY62147DV30LL	Industrial	–40°C to +85°C	
	Automotive-A	–40°C to +85°C	

Electrical Characteristics (Over the Operating Range)

Parameter	Description	Test Conditions		–45 Min.	–45 Typ.[5]	–45 Max.	–55/–70 Min.	–55/–70 Typ.[5]	–55/–70 Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V	2.0			2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V	2.4			2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V			0.4			0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70V			0.4			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3V	1.8		V_{CC} + 0.3V	V
		V_{CC} = 2.7V to 3.6V		2.2		V_{CC} + 0.3V	2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	–0.3		0.6	V
		V_{CC} = 2.7V to 3.6V		–0.3		0.8	–0.3		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	Ind'l	–1		+1	–1		+1	μA
			Auto-A[9]				–1		+1	μA
			Auto-E[9]				–4		+4	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	Ind'l	–1		+1	–1		+1	μA
			Auto-A[9]				–1		+1	μA
			Auto-E[9]				–4		+4	μA
I_{CC}	V_{CC} Operating Supply Current	f = f_{MAX} = 1/t_{RC}	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels		10	20		8	15	mA
		f = 1 MHz			1.5	3		1.5	3	mA
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.2V, V_{IN}≥V_{CC}–0.2V, V_{IN}≤0.2V) f = f_{MAX} (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), V_{CC} = 3.60V	Ind'l LL			8			8	μA
			Auto-A[9] LL						8	
			Auto-E[9] L						25	
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current — CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.60V	Ind'l LL			8			8	μA
			Auto-A[9] LL						8	
			Auto-E[9] L						25	

Notes:
6. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
7. $V_{IH(max.)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
8. Full device AC operation assumes a 100-μs ramp time from 0 to V_{CC}(min) and 200-μs wait time after V_{CC} stabilization.
9. Auto-A is available in –70 and Auto-E is available in –55.

[+] Feedback

Capacitance (for all packages)[10]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25°C$, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance[10]

Parameter	Description	Test Conditions	VFBGA	TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	72	75.13	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		8.86	8.95	°C/W

AC Test Loads and Waveforms[10]
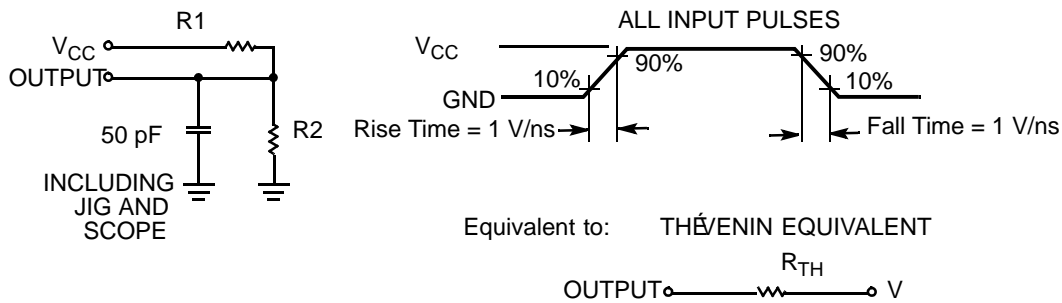
Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions		Min.	Typ.[5]	Max.	Unit
V_{DR}	V_{CC} for Data Retention			1.5			V
I_{CCDR}	Data Retention Current	$V_{CC}= 1.5V$ $\overline{CE} \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	L (Auto-E)			15	μA
			LL (Ind'l/Auto-A)			6	
t_{CDR}[10]	Chip Deselect to Data Retention Time			0			ns
t_R[12]	Operation Recovery Time			t_{RC}			ns

Data Retention Waveform[13]
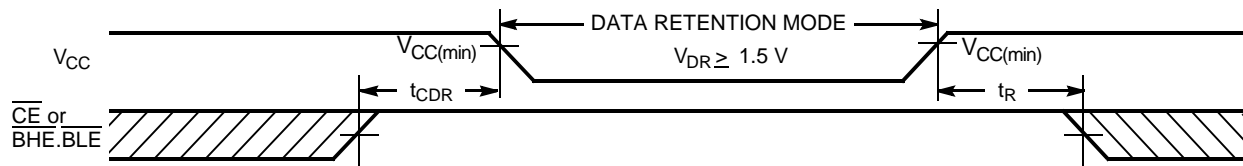
Notes:
10. Tested initially and after any design or process changes that may affect these parameters.
11. Test condition for the 45-ns part is a load capacitance of 30 pF.
12. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 100$ μs or stable at $V_{CC(min.)} \geq 100$ μs.
13. BHE.BLE is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

[+] Feedback

Switching Characteristics Over the Operating Range[14]

| Parameter	Description	45 ns[11]		55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address to Data Valid		45		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		45		55		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25		25		35	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[15]	5		5		5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[15, 16]		15		20		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[15]	10		10		10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[15, 16]		20		20		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		45		55		70	ns
t_{DBE}	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55		70	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z[15]	10		10		10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[15, 16]		15		20		25	ns
Write Cycle[17]								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	40		40		60		ns
t_{AW}	Address Set-up to Write End	40		40		60		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	35		40		45		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		40		60		ns
t_{SD}	Data Set-up to Write End	25		25		30		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[15, 16]		15		20		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[15]	10		10		10		ns

Notes:
14. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns (1 V/ns) or less, timing reference levels of $V_{CC(typ.)}$/2, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
15. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
16. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
17. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
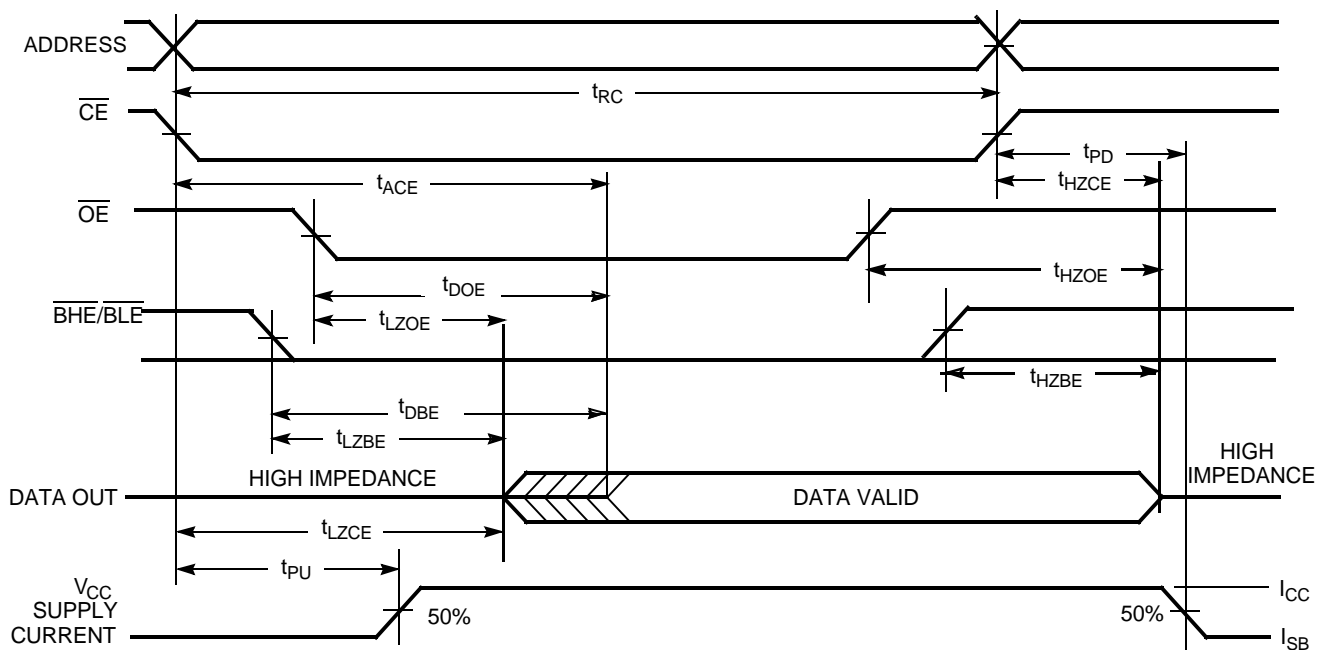
[+] Feedback

Switching Waveforms

Read Cycle 1 (Address Transition Controlled)[18, 19]
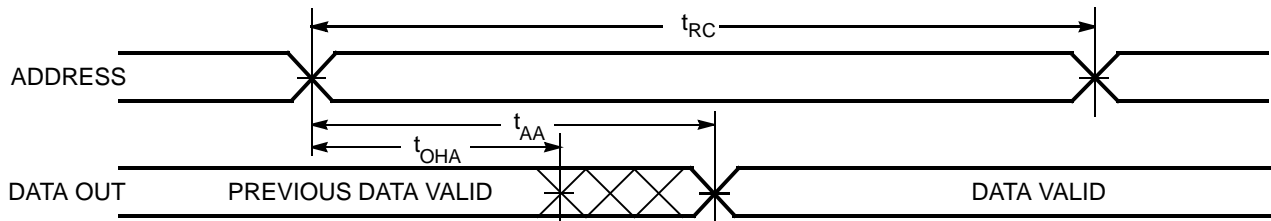
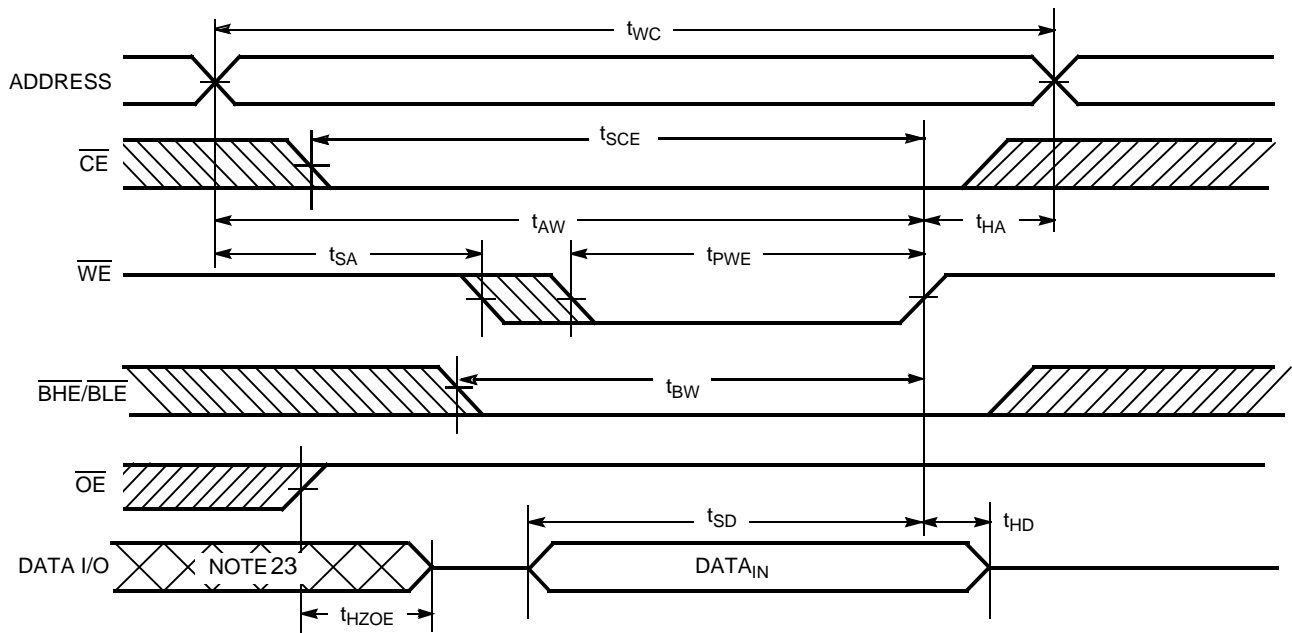

Read Cycle No. 2 ($\overline{OE}$ Controlled)[19, 20]

Notes:
18. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ and/or $\overline{BLE}$ = V_{IL}.
19. $\overline{WE}$ is HIGH for read cycle.
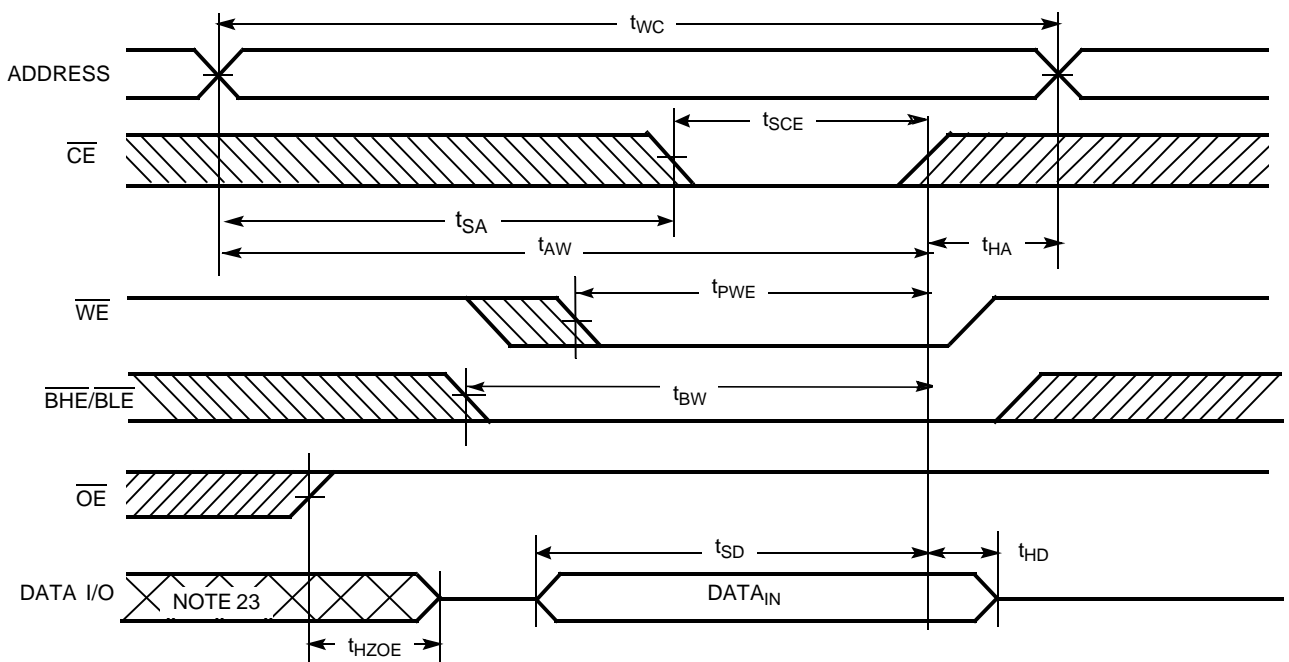20. Address valid prior to or coincident with $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 1 (WE Controlled)[17, 21, 22]

Write Cycle No. 2 (CE Controlled)[17, 21, 22]

Notes:
21. Data I/O is high impedance if $\overline{OE}$ = V$_{IH}$.
22. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ = V$_{IH}$, the output remains in a high-impedance state.
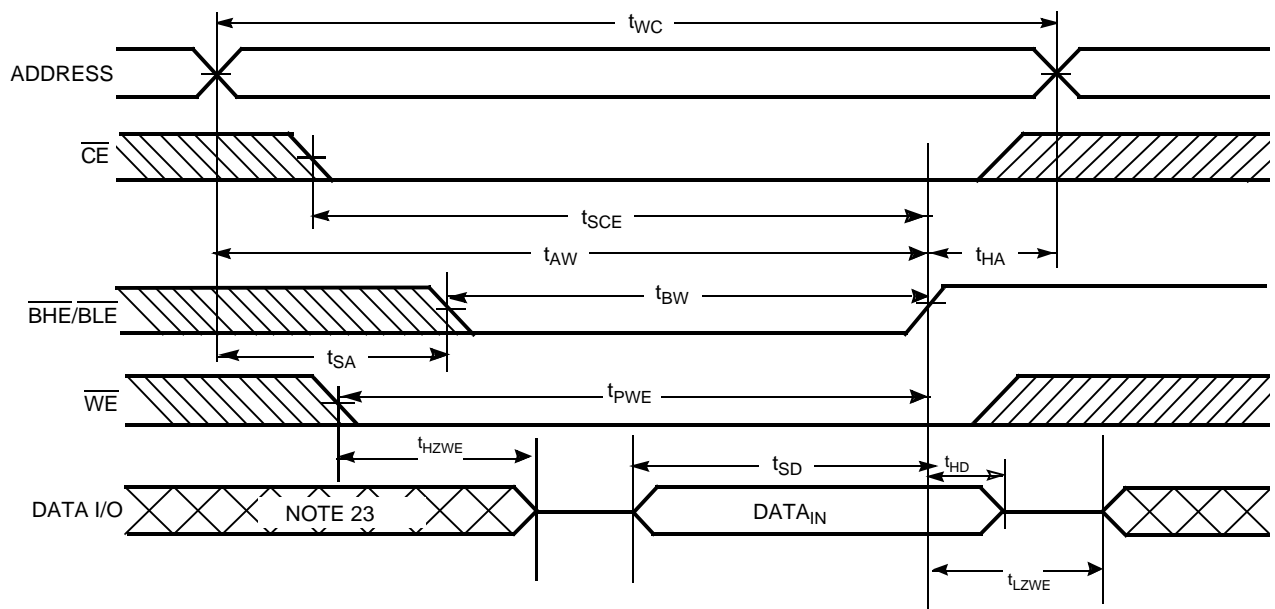23. During this period, the I/Os are in output state and input signals should not be applied.

[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)[22]
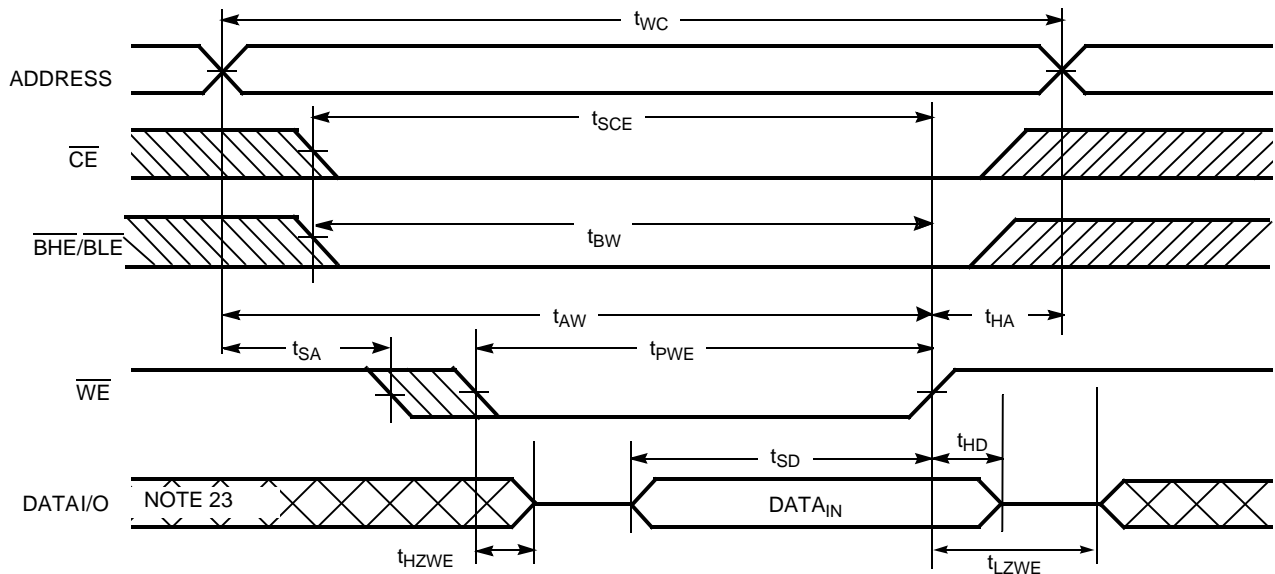
Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW)[22]

[+] Feedback

Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
X	X	X	H	H	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62147DV30LL-45BVXI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	Industrial
	CY62147DV30LL-45ZSXI	51-85087	44-pin TSOP II (Pb-free)	
55	CY62147DV30LL-55BVI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA	Industrial
	CY62147DV30LL-55BVXI		48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	
	CY62147DV30LL-55ZSXI	51-85087	44-pin TSOP II (Pb-free)	
	CY62147DV30L-55BVXE	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	Automotive-E
	CY62147DV30L-55ZSXE	51-85087	44-pin TSOP II (Pb-free)	
70	CY62147DV30LL-70BVI	51-85150	48-ball (6 mm × 8mm × 1 mm) VFBGA	Industrial
	CY62147DV30LL-70BVXA		48-ball (6 mm × 8mm × 1 mm) VFBGA (Pb-free)	Automotive-A

[+] Feedback

Package Diagram

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)
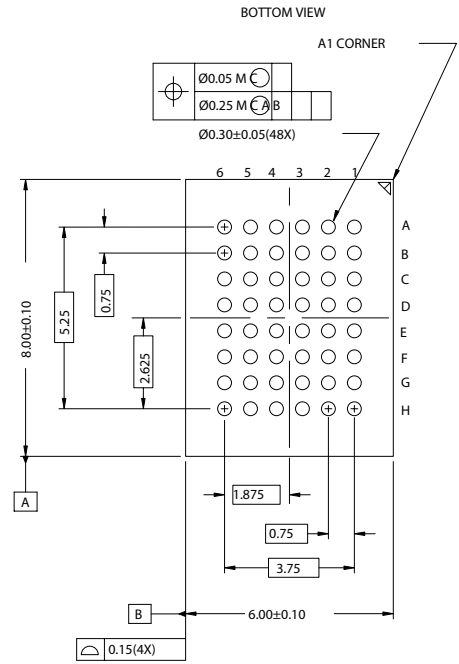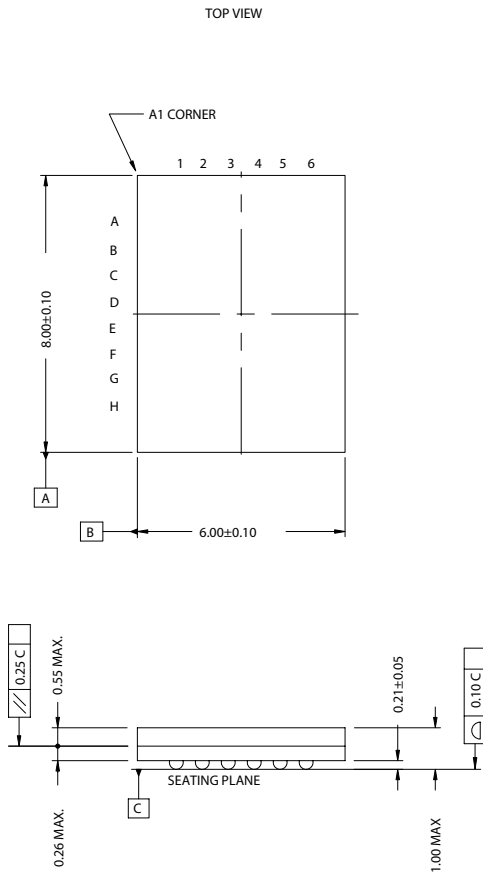
TOP VIEW

A1 CORNER

BOTTOM VIEW

A1 CORNER

51-85150-*D

[+] Feedback

Package Diagram (continued)

44-Pin TSOP II (51-85087)

DIMENSION IN MM (INCH)
MAX
MIN

TOP VIEW

PIN 1 I.D.

22   1

11.938 (0.470)
11.735 (0.462)

23   44

BOTTOM VIEW

10.262 (0.404)
10.058 (0.396)

EJECTOR PIN

0.800 BSC
(0.0315)

0.400(0.016)
0.300 (0.012)

BASE PLANE

18.517 (0.729)
18.313 (0.721)

0.10 (.004)

SEATING
PLANE

1.194 (0.047)
0.889 (0.035)

0.150 (0.0059)
0.050 (0.0020)

10.262 (0.404)
10.058 (0.396)

0°-5°

0.210 (0.0083)
0.120 (0.0047)

0.597 (0.0235)
0.406 (0.0160)
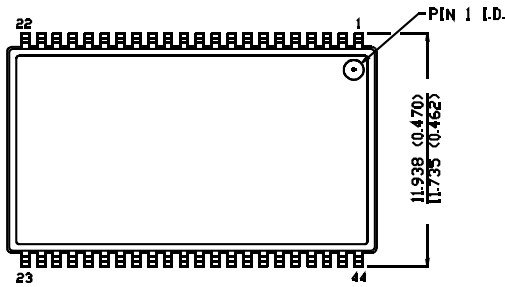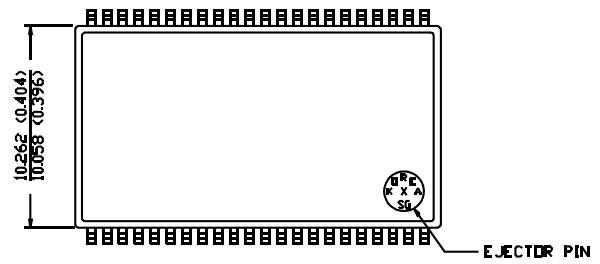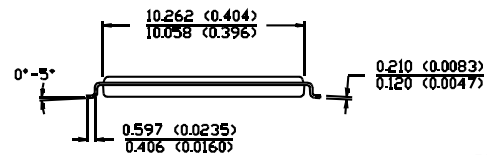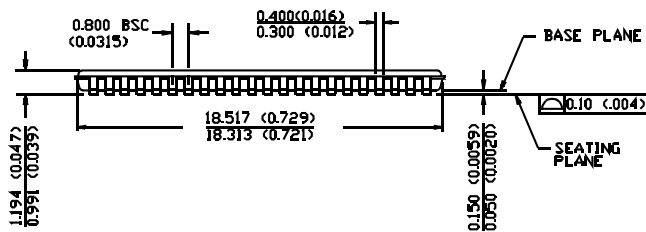
51-85087-*A

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[+] Feedback

Document History Page

Document Title:CY62147DV30 MoBL® 4-Mbit (256K x 16) Static RAM
Document Number: 38-05340

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	127481	06/17/03	HRT	New Data Sheet
*A	131010	01/23/04	CBD	Changed from Advance to Preliminary
*B	213252	See ECN	AJU	Changed from Preliminary to Final Added 70 ns speed bin Modified footnote 7 to include ramp time and wait time Modified input and output capacitance values to 10 pF Modified Thermal Resistance values on page 4 Added "Byte power-down feature" in the features section Modified Ordering Information for Pb-free parts
*C	257349	See ECN	PCI	Modified ordering information for 70-ns Speed Bin
*D	316039	See ECN	PCI	Added 45-ns Speed Bin in AC, DC and Ordering Information tables Added Footnote #10 on page #4 Added Pb-free package ordering information on page # 9 Changed 44-lead TSOP-II package name on page 11 from Z44 to ZS44 Standardized Icc values across 'L' and 'LL' bins
*E	330365	See ECN	AJU	Added Automotive product information
*F	498575	See ECN	NXR	Added Automotive-A range Added note# 9 on page# 3 Updated ordering information table

[+] Feedback